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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,330	TAKATORI ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *328,915*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The elements in Figs.1A, 1B, 2, 4 and 6 need to have descriptive label, in conformance with 37 CFR 1.84(n) and 1.84(o). For example, a descriptive label of "phase detector " should be inserted into 6 of Fig.1A to properly describe element.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

   In claim 1, line 3, delete "of input data" and insert "of an input data".

   In claim 1, line 7, delete "inputting data" and insert "inputting said input data".

   In claim 1, line 8, delete "estimating phase" and insert "estimating a phase".

   In claim 1, line 13, delete "said non-linear" and insert "said at least two non-linear". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-21 and 23-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 1, lines 8-9,

claim 5, line 9, claim 18, lines 5-7 and claim 23, line 10 recite the relationship between an input data, data sample and phase sample. The specification does not appear to clearly describe how the phase sample and data sample are produced. From the claims, it appears that the phase sample and data sample are derived from the input data. Is this correct? The specification does not describe in such a way to reasonably convey to one skilled in the art of how the phase and data samples are produced.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-4 and 18-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 18, lines 11 and 8, respectively, recite "a sign of recovered data", which is unclear as to what is meant by the sign of recovered data. Is this the data output of the phase error estimating step?

In claim 21, line 3, recites "a summed output" and further, in claim 18, line 13, recites "said summed output". It is unclear as whether the summed output recited in claim 21 is a different or the same output.

Claims 2-4 and 19-21 directly depend on claim 1 or 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 22 is rejected under 35 U.S.C. 102(b) as being anticipated by La Rosa et al. USP 5,247,544 (La Rosa).

Regarding claim 22, La Rosa discloses a receiver system (see Fig.1) comprising a receiver circuit (101); an antenna (105) in electronic communication with said receiver circuit; and a timing recovery system circuit (clock recovery, 127) in electronic communication with said receiver circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-7 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masenas et al. USP 6,614,316 B2 (Masenas) in view of Hill USP 6,031,428.

Regarding claim 5, Masenas teaches a timing recovery system (see Fig.2) to receive input data having a phase comprising: a phase locked loop to lock a phase of a local clock to the phase of said input data, said phase locked loop

receiving said input data and generating a phase locked loop output (which is a function of a PLL, note col.1, lines 39-52 and see Fig.2 having a loop (102,108,116,110 and 104 in Fig.2) and further teaches a first proportional path (102,106,114,116,110 and 104) with non-linear control to adjust the phase of said input data in response to a data pattern of said input data (note col.5, lines 22-52 wherein depending on the data of the input signal, phase is adjusted by the user-selected value of PM), said first proportional path receiving said input data and generating a first proportional path output (202). Masenas further teaches a system summing node (116).

However, Masenas does not teach a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of said input data, said second proportional path receiving said input data and generating a second proportional path output.

Hill teaches a timing recovery system (see Fig.1) comprising a second proportional path (10,12,14,16,18 and 20) with non-linear control to adjust the phase of said input data in response to an amplitude of said input data (wherein the phase detector,10, further shown in Fig.5 determines the peak amplitude, 52, to output gain control, note col.7, lines 44-46, and thus adjusts the phase, note col.7, lines 60-64), said second proportional path receiving said input data and generating a second proportional path output (output of 14), wherein the output is coupled to a system summing node (16).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Hill in the system of Masenas by coupling the second proportional path output (14 of Hill) to the system summing node (116 of Masenas) for the purpose of further considering amplitude or gain in adjusting the phase of the input data by adding the result at the summing node to control an oscillator in the timing recovery system.

Regarding claim 6, Masenas in view Hill teach all subject matter claimed, as applied to claim 5. Masenas, as explained previously, teaches wherein said data pattern of said input data causes said first proportional path to adjust said phase of said input data. However, Masenas does not explicitly teach wherein said input data is a string of zeros followed by a value of one in said input data. Considering that the high and low (note col.5, lines 30-31) is a one and a zero, respectively, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have said input data having a string of zeros followed by a value of one in said input data. Applicant has not disclosed that such input data provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with said input data having a different data pattern because regardless of the data pattern having a certain mixture of zeros and ones, it would have been detected.

Therefore, it would have been obvious to one of ordinary skill in this art to modify the system of Masenas to implement as such of receiving the a string of zeros followed by a value of one in said input data to obtain the invention as specified in claim.

Regarding claim 7, Masenas in view Hill teach all subject matter claimed, as applied to claim 5. Masenas further teaches wherein said phase locked loop further includes a phase detector (102) to determine said phase of said input data, said phase detector receiving said input data and generating a phase detector output (inc, dec); and a loop filter (108,112,114, note col.5, lines 37-40) to provide additional frequency characteristic to said phase detector output, said loop filter receiving said phase detector output and generating said phase locked loop output (output of 114).

Regarding claim 10, Masenas in view Hill teach all subject matter claimed, as applied to claim 5. Hill further teaches wherein said timing recovery system further includes an oscillator (20 in Fig.1) receiving said system summing node output (output of 16) and generating a final system output (output of 20).

Regarding claims 11-13, Masenas in view Hill teach all subject matter claimed, as applied to claim 10. Hill further teach wherein said oscillator is a VCO, as explained above. And further, the implementation of a DCO and DAC as an oscillator is well-known in the art. Therefore, it would have been obvious to one

skilled in the art at the time of the invention to use DCO and DAC as an oscillator for the purpose of designing a system using components which may be abundant in the market or designing using components that are cheaper to reduce the overall system cost.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masenas et al. USP 6,614,316 B2 (Masenas) in view of Hill USP 6,031,428 and Perrott et al. USP 6,630,868 B2 (Perrott).

Regarding claim 9, Masenas in view of Hill teach all subject matter claimed, as applied to claim 5, however, do not teach a third proportional path with non-linear control to reduce an accumulated phase error, said third proportional path receiving said input data and generating a third proportional path output, wherein said third proportional path output is summed by said system summing node. Perrott teaches a third proportional path (154,156,158,160 in Fig.3) with non-linear control to reduce an accumulated phase error (156, note col.5, lines 43-64), said third proportional path receiving said input data and generating a third proportional path output (180), wherein said third proportional path output is summed by a system summing node (150). Therefore, it would have been obvious to one skilled in the art at the time of the invention to couple the third proportional path of Perrott receiving the input data of Masenas and outputting the third proportional path output (180) coupled to the system summing node of

Masenas for the purpose of removing jitter in the PLL and prevent from losing any data from the input data, as taught by Perrott (note col.2, lines 18-26).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masenas et al. USP 6,614,316 B2 (Masenas) in view of Hill USP 6,031,428 and Ogawa USP 5,574,757.

Regarding claim 17, Masenas in view of Hill teach all subject matter claimed, as applied to claim 5. However, Masenas in view of Hill do not teach wherein at least one of said first proportional path and said second proportional path include at least one hold off counter.

Ogawa teaches a PLL circuit comprising a hold off counter (10 in Fig.2).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to include the hold off counter of Ogawa in the first or second proportional path of Masenas in view of Hill for the purpose of designing a robust system by generating an accurate clock signal during some failure and deterioration of input clock signals, as taught by Ogawa (note col.2, lines 12-20).

9. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill USP 6,031,428 in view of Roberts et al. USP 6,735,259 B1 (Roberts).

Regarding claim 18, Hill teaches a timing recovery system (see Fig.1) to estimate a phase error (10, also shown in Fig.4, output of 40) and correlate or match (note col.6, lines 50-63) said phase error (output of 40) with a sign of recovered data

(first input to 42); filter said correlated phase error by a loop filter to generate an output (14); sum (16) said output with a path output from at least one non-linear path (22,24,26) to generate a summed output (output of 16); and convert said summed output into clock information (output of 20).

However, Hill does no teach estimating a phase error based on a data sample from both a center of a data eye of input data and from a phase sample from said input data half-a-baud later in time.

Roberts teaches estimation of a phase error based on a data sample from both a center of a data eye of input data (see Fig.2, optimum timing T_{OPT}) and from a phase sample from said input data (delayed version between T- and T_{OPT} or between T+ and T_{OPT}, note col.9, lines 16-28). Therefore, it would have been obvious to one skilled in the art at the time of the invention to implement the step of estimating the phase error of Roberts in the system of Hill for the purpose of increasing the accuracy of the timing recovery of the system (note col.9, lines 11-15). And although Roberts does not explicitly teach that the phase sample from said input data is half-a-baud later in time, Roberts suggests that the clock recovery (4) may generate plurality of clock signals having a unique phase offset (note col.9, lines 17-19). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the phase sample from said input data is half-a-baud later in time. Applicant has not disclosed that the limitation provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected

Applicant's invention to perform equally well with the phase sample delayed by other unique phase offset because the processor would know the delay between the center of the eye and the clock signal generated by the clock recovery. Therefore, it would have been obvious to one of ordinary skill in this art to implement the invention as specified in claim. And further, although Hill in view of Roberts do not explicitly disclose that the timing recovery system comprises a machine-readable storage medium having a machine-readable program code, stored on the machine-readable storage medium, the machine-readable program code having instructions to implement the steps above, it is well-known to one skilled in the art to implement timing recovery processes in a computer.

Regarding claims 19 and 20, Hill in view of Roberts teach all subject matter claimed, as applied to claim 18. Hill further teaches multiplying said correlated phase error by a gain (12 in Fig.1) prior to filtering (14) said correlated phase error by said loop filter.

Regarding claim 21, Hill in view of Roberts teach all subject matter claimed, as applied to claim 18. Hill further teaches summing said output (16) with a non-linear paths to generate the summed output (output of 16). Although Hill does not explicitly teach having three non-linear paths to be summed, it would have been obvious to one skilled in the art at the time of the invention to implement as such for the purpose of increasing the conditions to adjust the phase, as

explained previously (such conditions as detection of data pattern, taught by Masenas and accumulated error, taught by Perrott).

10. Claims 23-25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over La Rosa et al. USP 5,247,544 (La Rosa) in view of Masenas et al. USP 6,614,316 B2 (Masenas) and Hill USP 6,031,428.

Regarding claim 23, La Rosa teaches all subject matter claimed, as applied to claim 22. However, La Rosa does not explicitly teach the elements of a phase locked loop, first and second proportional path and a system summing node. Masenas teaches a timing recovery system (see Fig.2) to receive input data having a phase comprising: a phase locked loop to lock a phase of a local clock to the phase of said input data, said phase locked loop receiving said input data and generating a phase locked loop output (which is a function of a PLL, note col.1, lines 39-52 and see Fig.2 having a loop (102,108,116,110 and 104 in Fig.2) and further teaches a first proportional path (102,106,114,116,110 and 104) with non-linear control to adjust the phase of said input data in response to a data pattern of said input data (note col.5, lines 22-52 wherein depending on the data of the input signal, phase is adjusted by the user-selected value of PM), said first proportional path receiving said input data and generating a first proportional path output (202). Masenas further teaches a system summing node (116).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the phase locked loop, first proportional path and the system summing node in the timing recovery system circuit of La Rosa for the purpose of increasing the control of the system by allowing the user to adjust loop dynamics, and also to increase the signal to noise ratio of the system (note col.2, lines 14-23).

However, La Rosa in view of Masenas do not teach a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of said input data, said second proportional path receiving said input data and generating a second proportional path output.

Hill teaches a timing recovery system (see Fig.1) comprising a second proportional path (10,12,14,16,18 and 20) with non-linear control to adjust the phase of said input data in response to an amplitude of said input data (wherein the phase detector,10, further shown in Fig.5 determines the peak amplitude, 52, to output gain control, note col.7, lines 44-46, and thus adjusts the phase, note col.7, lines 60-64), said second proportional path receiving said input data and generating a second proportional path output (output of 14), wherein the output is coupled to a system summing node (16).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Hill in the system of La Rosa in view of Masenas by coupling the second proportional path output (14 of Hill) to the system summing node (116 of Masenas) for the purpose of further considering

amplitude or gain in adjusting the phase of the input data by adding the result at the summing node to control an oscillator in the timing recovery system.

Regarding claim 24, La Rosa in view of Masenas and Hill teach all subject matter claimed, as applied to claim 23. Masenas, as explained previously, teaches wherein said data pattern of said input data causes said first proportional path to adjust said phase of said input data. However, Masenas does not explicitly teach wherein said input data is a string of zeros followed by a value of one in said input data. Considering that the high and low (note col.5, lines 30-31) is a one and a zero, respectively, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have said input data having a string of zeros followed by a value of one in said input data. Applicant has not disclosed that such input data provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with said input data having a different data pattern because regardless of the data pattern having a certain mixture of zeros and ones, it would have been detected.

Therefore, it would have been obvious to one of ordinary skill in this art to modify the system of Masenas to implement as such of receiving the a string of zeros followed by a value of one in said input data to obtain the invention as specified in claim.

Regarding claim 25, La Rosa in view of Masenas and Hill teach all subject matter claimed, as applied to claim 23. Masenas further teaches wherein said phase locked loop further includes a phase detector (102) to determine said phase of said input data, said phase detector receiving said input data and generating a phase detector output (inc, dec); and a loop filter (108,112,114, note col.5, lines 37-40) to provide additional frequency characteristic to said phase detector output, said loop filter receiving said phase detector output and generating said phase locked loop output (output of 114).

Regarding claim 28, La Rosa in view of Masenas and Hill teach all subject matter claimed, as applied to claim 23. Hill further teaches wherein said timing recovery system further includes an oscillator (20 in Fig.1) receiving said system summing node output (output of 16) and generating a final system output (output of 20).

11. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over La Rosa et al. USP 5,247,544 (La Rosa) in view of Masenas et al. USP 6,614,316 B2 (Masenas) and Hill USP 6,031,428 and in further view of Perrott et al. USP 6,630,868 B2 (Perrott).

Regarding claim 27, La Rosa Masenas in view of Hill teach all subject matter claimed, as applied to claim 23, however, do not teach a third proportional path with non-linear control to reduce an accumulated phase error, said third proportional path receiving said input data and generating a third proportional

path output, wherein said third proportional path output is summed by said system summing node.

Perrott teaches a third proportional path (154,156,158,160 in Fig.3) with non-linear control to reduce an accumulated phase error (156, note col.5, lines 43-64), said third proportional path receiving said input data and generating a third proportional path output (180), wherein said third proportional path output is summed by a system summing node (150). Therefore, it would have been obvious to one skilled in the art at the time of the invention to couple the third proportional path of Perrott receiving the input data of Masenas and outputting the third proportional path output (180) coupled to the system summing node of Masenas for the purpose of removing jitter in the PLL and prevent from losing any data from the input data, as taught by Perrott (note col.2, lines 18-26).

12. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over La Rosa et al. USP 5,247,544 (La Rosa) in view of Masenas et al. USP 6,614,316 B2 (Masenas) and Hill USP 6,031,428 in further view of Ogawa USP 5,574,757.

Regarding claim 32, Masenas in view of Hill teach all subject matter claimed, as applied to claim 23. However, Masenas in view of Hill do not teach wherein at least one of said first proportional path and said second proportional path include at least one hold off counter.

Ogawa teaches a PLL circuit comprising a hold off counter (10 in Fig.2).

Therefore, it would have been obvious to one skilled in the art at the time of the

invention to include the hold off counter of Ogawa in the first or second proportional path of Masenas in view of Hill for the purpose of designing a robust system by generating an accurate clock signal during some failure and deterioration of input clock signals, as taught by Ogawa (note col.2, lines 12-20).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
6/26/05

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER

6/28/05